Cont A2

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being [gated] coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being [gated] coupled to said first and second inverters by the inverted enable signal.

4. (Amended) The circuit of claim 3, wherein said first voltage source is [gated] coupled by a P-channel transistor responsive to the enable signal.

5. (Amended) The circuit of claim 3, wherein said second voltage source is [gated] coupled by a N-channel transistor responsive to the inverse of the enable signal.

6. (Amended) The circuit of claim 3, wherein said first voltage source is [gated] coupled by an N-channel transistor responsive to the enable signal.

7. (Amended) The circuit of claim 3, wherein said second voltage source is [gated] coupled by an P-channel transistor responsive to the inverse of the enable signal.

A3 Sub B3

9. (Amended) The circuit of claim 8, wherein each of said first and second input buffer circuits comprises:

an input for receiving [an] one of said first and second external signals;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said inputs, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

13. (Amended) The circuit of claim 12, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter [gating] coupling the output of said first and second driver inverters to a predetermined voltage.

21. (Amended) The circuit of claim 20, wherein each of said first and second input buffer circuits comprises:

an input for receiving [an] one of said first and second external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

25. (Amended) The circuit of claim 24, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter [gating] coupling the output of said first and second driver inverters to a predetermined voltage.

28. (Amended) The circuit of claim 27, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being [gated] coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being [gated] coupled to said inverters by the inverted enable signal.

29. (Amended) The circuit of claim 28, wherein said first voltage source is [gated] coupled by a P-channel transistor responsive to the enable signal.

cont A7

30. (Amended) The circuit of claim 28, wherein said second voltage source is [gated] coupled by a N-channel transistor responsive to the inverse of the enable signal.

31. (Amended) The circuit of claim 28, wherein said first voltage source is [gated] coupled by an N-channel transistor responsive to the enable signal.

32. (Amended) The circuit of claim 28, wherein said second voltage source is [gated] coupled by an P-channel transistor responsive to the inverse of the enable signal.

A8 Sub B11

34. (Amended) The circuit of claim 33, wherein each of said first and second input buffer circuits comprises:

an input for receiving [an] one of said first and second external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

A9

37. (Amended) The circuit of claim 36, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter [gating] coupling the output of said first and second driver inverters to a predetermined voltage.

Sub D1

38. (Amended) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving [an] one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

40. (Amended) The circuit of claim 39, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being [gated] coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being [gated] coupled to said inverters by the inverted enable signal.

41. (Amended) The circuit of claim 40, wherein said first voltage source is [gated] coupled by a P-channel transistor responsive to the enable signal.

42. (Amended) The circuit of claim 40, wherein said second voltage source is [gated] coupled by a N-channel transistor responsive to the inverse of the enable signal.

43. (Amended) The circuit of claim 40, wherein said first voltage source is [gated] coupled by an N-channel transistor responsive to the enable signal.

CONT A10

44. (Amended) The circuit of claim 40, wherein said second voltage source is [gated] coupled by an P-channel transistor responsive to the inverse of the enable signal.

A11

47. (Amended) The circuit of claim 46, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter [gating] coupling the output of said first and second driver inverters to a predetermined voltage.

SUB D1

48. (Amended) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving [an] one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line; and

a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

50. (Amended) The circuit of claim 49, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being [gated] coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being [gated] coupled to said inverters by the inverted enable signal.

51. (Amended) The circuit of claim 50, wherein said first voltage source is [gated] coupled by a P-channel transistor responsive to the enable signal.

Amd A12 Sub D1

52. (Amended) The circuit of claim 50, wherein said second voltage source is [gated] coupled by a N-channel transistor responsive to the inverse of the enable signal.

53. (Amended) The circuit of claim 50, wherein said first voltage source is [gated] coupled by an N-channel transistor responsive to the enable signal.

54. (Amended) The circuit of claim 50, wherein said second voltage source is [gated] coupled by an P-channel transistor responsive to the inverse of the enable signal.

A13 Sub D1

56. (Amended) The circuit of claim 55, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter [gating] coupling the output of said first and second driver inverters to a predetermined voltage.

REMARKS

The application has been carefully reviewed in light of the Office Action dated September 15, 2000. Claims 3-7, 13, 25, 28-32, 37, 40-44, 47, 50-54 and 56 have been amended for clarity. Claims 1-56 and 82-98 are now pending in this case.

Claims 9, 10, 15, 16-25, 34, 35 and 38-56 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

Claims 9, 10, 21-22, 34-35, 38-47, and 48-56 stand rejected because the disclosure does not provide or show the limitation "a differential amplifier" to support the